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Description

METHOD OF FORMING A GATE STRUCTURE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method of forming a gate structure, and more particularly, to a method for preventing the word line and the bit line from generating short circuits.

[0003] 2. Description of the Prior Art

[0004] Dynamic random access memory (DRAM) is composed of many memory cells, and each memory cell has a metal oxide semiconductor (MOS) transistor and a capacitor. The gate of the MOS transistor (also known as word line) serves as a switch of the transistor, while the drain or the source is connected to a bit line for writing and erasing data.

[0005] Refer to Fig. 1 and Fig. 2, which are schematic diagrams

illustrating a method of forming a controlling gate of a DRAM according to the prior art. As shown in Fig. 1, first a substrate 10 having at least a stacked gate 12 is provided. The stacked gate 12 has a gate insulating layer 14, a polysilicon layer 16, a silicate layer 18, and a cap layer 20.

[0006] As shown in Fig. 2, a chemical vapor deposition (CVD) process is performed to form a silicon nitride layer on the substrate 10. Then an anisotropic process is performed to form a spacer 22 on the walls of the stacked gate 12. After that, an implantation process is performed to form a drain (not shown) and a source (not shown) in the substrate 10.

[0007] After forming the stacked gate 12, the prior art method further comprises the steps of forming a bit line. Refer to Fig. 3 to Fig. 5 which are schematic diagrams illustrating a method of forming the bit line. As shown in Fig. 3, a barrier layer 24 is deposited on the substrate 10 and on the stacked gate 12 after forming the stacked gate 12. Then a borophosphosilicate glass (BPSG) layer 26 is deposited on the barrier layer 24, and a flow process is performed to planarize the BPSG layer 26. Finally, a chemical mechanical polishing (CMP) process is performed to remove the BPSG layer 26 over the top surface of the cap layer 20. The

function of the barrier layer 24 is to prevent the ions of the BPSG layer 26 from diffusing to the substrate 10 during the flow process.

[0008] As shown in Fig. 4, a dielectric layer 28 (such as a TEOS layer) is deposited on the stacked gate 12. Then a photo-etching process is performed to remove parts of the dielectric layer 28, the BOSG layer 26, and the barrier layer 24 for forming a contact hole 30.

[0009] Finally as shown in Fig. 5, a bit line 32 is formed and electrically connected to the drain (not shown) or the source (not shown).

[0010] The prior art method utilizes the spacer to prevent the word line and the bit line from generating short circuits. As the integration of semiconductor elements increases and the dimension decreases day by day, however, the spacer is easily destroyed when forming the contact hole due to misalignment. The bit line and the silicate layer are easily short circuited under this condition, especially when the dimension of the semiconductor process is lower than 0.11 micrometers.

SUMMARY OF INVENTION

[0011] It is therefore a primary objective of the claimed invention to provide a method of forming a controlling gate of a

DRAM for solving the above-mentioned problems.

[0012] According to the claimed invention, a method of forming a controlling gate of a DRAM is disclosed. The method comprises: providing a substrate having at least a stacked gate, the stacked gate comprising a gate insulating layer, a polysilicon layer, a silicate layer, and a cap layer; depositing a sacrificial layer on the stacked gate; etching back the sacrificial layer to expose the cap layer and an upper portion of the silicate layer; removing a portion of the exposed silicate layer to form a recess; removing the sacrificial layer; filling a silicon nitride layer in the recess; and forming a spacer on walls of the stacked gate.

[0013] It is an advantage of the claimed invention that a recess is formed in the upper portion of the silicate layer, and a silicon nitride layer is filled intothe recess. Therefore the short circuit problem is effectively avoided.

[0014] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0015] Fig. 1 and Fig. 2 are schematic diagrams illustrating a

method of forming a controlling gate of a DRAM according to the prior art.

[0016] Fig. 3 to Fig. 5 are schematic diagrams illustrating a method of forming a bit line according to the prior art.

[0017] Fig. 6 to Fig. 9 are schematic diagrams illustrating a method of forming a controlling gate of a DRAM according to the present invention.

Detailed Description

[0018] Refer to Fig. 6 to Fig. 9, which are schematic diagrams illustrating a method of forming a controlling gate of a DRAM according to the present invention. First as shown in Fig. 6, a substrate 50 has at least a stacked gate 52. The stacked gate 52 comprises a gate insulating layer 54, a polysilicon layer 56, a silicate layer 58, and a cap layer 60. The polysilicon layer 56 is composed of doped polysilicon, the silicate layer 58 is composed of silicon tungsten (Wsi_x), and the cap layer 60 is composed of silicon nitride. It has to be noted that the silicate layer 58 is the word line of DRAM.

[0019] As shown in Fig. 7, a sacrificial layer 62 is deposited on the substrate 50 and the stacked gate 52. Then an etching process is performed to remove parts of the sacrificial layer 62 for exposing the cap layer 60 and the upper por-

tion of the silicate layer 58.

[0020] As shown in Fig. 8, an anisotropic etching process is performed to remove parts of the exposed silicate layer 58 for forming a recess 64. Then the remaining sacrificial layer 62 is removed.

[0021] Finally as shown in Fig. 9, a silicon nitride film 66 is deposited to fill up the recess 64, and an etching process is performed to remove the silicon nitride film 66 outside the recess 64. Then another silicon nitride layer is deposited on the stacked gate 52, and another etching process is performed to form a spacer 68 on the walls of the stacked gate 52. It is worth noticing that the step of filling the recess and the step of forming the spacer 68 are respectively carried out by a deposition process and an etching process. However, these two steps can be carried out by a single deposition process and a single etching process in the present invention.

[0022] In addition, the method of the present invention further comprises steps of forming the bit line. However, since the steps of the present invention are similar to the steps of the prior art, details are not given here.

[0023] Comparing to the prior art, the method of the present invention forms a recess in the upper portion of the silicate

layer, and fills a silicon nitride layer as a passivation layer, such that the word line and bit line will not short circuit. Furthermore, since the silicon nitride layer only occupies a portion of the silicate layer, thus the conductivity of the silicate layer is not reduced.

[0024] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.